Section 3:

Schematic Rules

EWS SCHEMATIC RULES AND CONVENTIONS

INTRODUCTION

The following rules are generic and apply to all schematics captured on any engineering workstation (EWS) such as DAISY, MENTOR, or VALID system or any other EWS system used to generate an AMCC-readable netlist for submission to AMCC.

For EWS-Specific schematic rules and procedures, refer to the appropriate Design Manual (or Submissions Guidelines Document), Volume II, Section 7.

The generic rules should also be reviewed by those submitting blueprints to AMCC in cases where AMCC is to do the design implementation, or when generating a LASAR 6 net list for submitting to AMCC. They should be followed as closely as possible, especially in the areas of naming conventions, to ensure compatibility between the blueprints and the captured macro-based schematics.

BORDER

- Use an AMCC border on all schematic pages.
- MENTOR: If a different border is required consult Volume II, Section 7 for instructions and consult AMCC. Documentation on the border will be required in the design submission.
- All pages MUST be commented with a page number, and all page numbers should be sequential. Follow the EWS-specific rules (Volume II, Section 7) regarding page names for hierarchical or nested schematics. The last page should be clearly identified, (e.g., page 10 of 10).

CHIP MACRO

- Every circuit MUST use a chip macro. The chip macro identifies the specific array, ECL type, I/O mode, and provides the AMCC MacroMatrix ERC software with array-specific parameters. AMCC prefers that the chip macro be placed on page one of a design. Its location is page-independent.

CHIP MACRO PARAMETERS

- The required chip macro parameters MUST be defined. Refer to the MacroMatrix User's Guide for more detail.
  - PRODUCT_NAME Required; The AMCC-assigned name.
  - DEVICE_NUMBER Required; The AMCC-assigned number.
  - PRODUCT_GRADE Required; MIL or COM for military or commercial. DO NOT USE COM4 OR COM5.
  - POWER_SUPPLY This is an optional parameter. The value can be STD4 (-4.5V), STD5 (-5.2V) or 5VREF (+5V) and applies to the ECL supply.

CHIP MACRO PINS

- Chip macro input pins MUST be attached to the global ground. This procedure is EWS-specific. Refer to Volume II, Section 7 for the exact method of specifying that a pin is to be connected to "GROUND".

  For visual clarity, the wires should point up for all V_{CC} supplies and point down for all V_{EE} supplies (GND for +5V circuits).

- If power and ground need to be rotated, refer to Volume II, Section 7 for EWS-specific schematic rules and procedures.

- Chip macro output pins labeled Y **MUST** be terminated.

- Bipolar chip macro output pins labeled VTA may be terminated, if not required by any BIxx macros. If BIxx macros with VTA inputs are used on the circuit, then the chip macro VTA output pin is routed to these pins.

FIXED POWER AND GROUND

- Chip macros contain the pad number for all fixed power and ground pads for a given array.

ADDED POWER AND GROUND

- When the number of power and ground pads needs to be increased due to simultaneously switching outputs, 3-state enable-drivers, or for added noise immunity, added power and ground macros must be used.

- The added power and ground macros must be individually placed on the schematics by the designer. Refer to the macro library for the appropriate macros. Q20000, Q14000, Q5000 and Q3500 Series use: ITPWR, ITGND, IEVCC.

- AMCC prefers that you place all power and ground macros with the circuit chip macro on page 1 of the schematics. Start the design on page 2.

POWER AND GROUND MACROS - PINS

- Wire the power and ground macro inputs and outputs in the same manner as described for the chip macro. Inputs are named ground and outputs are terminated.

MACROS

- Only AMCC-created macros (MENTOR, DAISY, VALID) and EWS-specific connectors and terminators (DAISY, VALID) may be used on any schematic. For MENTOR, AMCC connectors and terminators MUST be used.
- Only released macros may be used in a design. For custom logic, please consult AMCC.
- EWS system primitives may not appear on a schematic.
- Rotation: the conventional logic flow on the page is from left (input) to right (output). AMCC prefers that rotation of macros is kept to a minimum to maintain this flow convention.
- All schematic objects (macros, wires, connectors, terminators, busses, blocks, etc.) MUST be spaced AT LEAST 2 grid positions apart, leaving enough room for a readable note to fit between them.
- Do not overlap macros, place on top of one another, or overcrowd so that they touch in any way.
- Do not wire through macros, blocks, cells, etc.
- The schematic MUST BE HUMAN READABLE - logic should be functionally grouped on the same or sequential schematic page(s).

USER-DEFINED UNIQUE (INSTANCE; OCCURRENCE) NAMES

- All macros MUST be given unique user-defined names in a flat design. Follow EWS-specific naming rules for nested or hierarchical designs (refer to Volume II, Section 7).
- All user-defined instance names are limited to a maximum of six (6) characters in length. Instance names are user-defined occurrence names of macros, cells, blocks, etc.
- All user-defined signal names are limited to a maximum of eight (8) characters in length.
- User-defined subscripted names, nested and hierarchy names, MUST follow the EWS-specific rules (Volume II, Section 7).
- All user-defined names in a circuit MUST be composed of alphanumeric characters (A-Z, 0-9). Short, meaningful names are recommended.
- All user-defined names may begin with a letter or a number.
- User-defined names MUST NOT contain spaces or special characters.
- Do not use duplicate names, AMCC macro names, or EWS connector names as unique signal or as unique instance names. All names MUST be unique within a circuit.
- Do not use keywords such as INPUT, OUTPUT, MODE, etc. as a name. Refer to the MacroMatrix User's Guide, Volume II, Section 8 for a list of reserved words.
- Grounds and terminators are not given user-defined names.
- WIREORs, if they exist in the macro library, are treated as any other AMCC macro and must be named.

MACRO NAMING CONVENTION

- AMCC PREFERS that you use the following naming conventions for assigning unique user-defined instance (occurrence) names to macros:

User-name FORMAT:	Macro class or type:
Axxxxx	Adder (ADxx, ADDxx series)
Bxxxxx	Buffer (BExx, BIxx series)
BDxxxx	Bipolar bi-directional I/O macros (UTxx, UExx, UKxx)
CHIP00	Chip Macro
COMxxx	Comparator (MSI)
CGxxxx	Carry-propagate (MSI)
CNTxxx	Counter
DRxxxx	Decoder (DExx series)
EIxxxx	ECL input (IExx, IPxx)
EOxxxx	ECL output (OExx, OPxx, OKxx, OQxx)
EGxxxx	EXOR/EXNOR (EXxx series)
Fxxxxx	Flip/flop (FFxx series)
Gxxxxx	Gate (GTxx series)
GNDTxx	TTL GROUND (ITGND)
GNDExx	ECL GROUND (IEGND)
Lxxxxx	Latch (LAxx series)
Mxxxxx	MUX (MXxx series)
PWRxxx	TTL VCC; (All Bipolar arrays);
MEMxxx	Memory module (RAMxx series)
RGxxxx	Register (REG00, REGxx series)
TIxxxx	TTL input (ITxx)
TOxxxx	TTL output (OTxx)
Wxxxxx	Wire-OR

Where: xxx, xxxx, and xxxxx indicate that from 1 up to 5 additional characters (usually digits) may be added to form a unique name (M00001, LA09, etc.).

Suggestion: include the page number as one of the digits used in a macro name (such as the first digit, FF1000 is FF000 on page 1) to help reduce duplicate names across multiple pages. They are difficult to debug.

NAMING SIGNALS

- The following signals MUST be given unique user-defined names:
  - All off-chip signals; wires attached to I/O macro PAD pins and external connectors.
  - All page-to-page (inter-page) signals; wires attached to page connectors.
  - All on-page signals; wires attached to intra-page connectors;
  - All signals in a critical path or in a path which will be examined by the at-speed or AC simulations using Front- and Back-Annotation delay files.
  - All 3-state enable control signals or bidirectional macro enable signals; wires attached to the enable pins.

Note that a signal [line] = a wire or wire-net on the EWS schematic.

UNUSED INTERNAL MACRO INPUT PINS (NON-PRIMARY INPUTS)

- All unused internal macro input pins are attached to the global ground ("GROUND" for all bipolar, BiCMOS I/O or "V_{DD}" (HIGH) or "V_{SS}" (LOW) for internal BiCMOS).

This procedure is EWS-specific. Refer to Volume II, Section 7 for the exact method of specifying that a pin is to be connected to "GROUND", "V_{DD}", or "V_{SS}".

- Bipolar: Exceptions to the above are those macros with pin hook-up restrictions. Be certain that all macro input pins that must be driven by a macro are driven and are not tied to "GROUND". In cases where an invariant signal is desired, internal buffer-drivers may be used to drive up to 32 static loads.
  For 1-4 loads: Use a simple L-option OR/NOR gate macro
  For 4-9 loads: Use a simple S-option OR/NOR gate macro
  For 10-32 loads: Use the static driver (HI/LOW) macro.

UNUSED INTERNAL MACRO OUTPUT PINS (NON-PRIMARY OUTPUTS)

- All unused internal macro output pins MUST be terminated.

CONNECTORS

- All chip I/O signals MUST use a primary input, primary output or primary bidirectional connector.
- All page signals MUST use page connectors with comments as to source page (for input), destination page (for output). For the VALID EWS, refer to Volume II, Section 7.
- All intra-page signals (a signal broken up on the same page for clarity is an intrapage signal) must use connectors. For the VALID EWS, refer to Volume II, Section 7. Minimize on-page breaks as they are hard to read.

SIMULTANEOUSLY SWITCHING OUTPUTS

- The SWGROUP macro parameter MUST be used for all simultaneously switching outputs. This will allow a correct I/O list to be generated and enable power/ground ERC checking. Refer to Volume II, Section 7 for EWS-specific information on how to attach the parameter and to Section 8 for its use in the ERCs. The parameter value must be visible on the schematic.

FAN-OUT LOAD DERATING

- Fan-out load limits for all clock, timing and distortion-sensitive paths that are to be derated must use the fan out derating NET parameter, FOD. Refer to Volume II, Section 7 for EWS-specific instructions on how to attach the parameter and to Section 8 for its use in the Fan-out ERC. The parameter value must be visible on the schematic.

LABELING CRITICAL PATHS

- Critical paths should be clearly identified on the schematics via notes. AMCC requires that one set of schematics be marked, with a highlighter or pen, to show all critical paths that will be examined during timing verification.

AMCC NON-EWS SCHEMATIC REQUIREMENTS
GENERIC

- AMCC must be provided with three (3) copies of the customer's logic diagrams or schematics, one of which is marked to show the critical and performance-sensitive paths, including paths to be tested with AC Test vectors.

- Schematics must be labeled as any blueprint with the following:
    - Company name
    - Circuit name
    - AMCC circuit name
    - PO # (if known)
    - AMCC array
    - Designer's name
    - Date
    - Page number
    - Revision level

- Schematics should be freely, extensively commented for clarity

- If possible, follow the EWS schematic conventions in Section 3.

- Complete the I/O list using the format described for the AMCCIO.LST, including simultanesouly switching outputs. Simultaneously switching outputs must be documented on the array resource checklist. Simultaneously switching outputs are those which switch within one logic device propagation delay of one another (are close enough to cause interference).

- Supply the additional information required for AMCCPKG.LST, including frequency for TTL I/O operating at > 50MHz and ECL I/O operating at > 100MHz. Include system loading and the desired package.

- Desired signal names should be indicated for all chip inputs and outputs and any other paths of interest. Current EWS/ERC conventions require that signal names be limited to eight alphanumeric characters, contain no special characters, and be unique within the circuit. Macro occurrence and other instance names are limited to 6 characters. No component names may be duplicated as signal names.

- Inter-page signals (page-to-page connections) MUST be commented on the schematics as to the pages that the signals connect to, either which pages they come from (for inputs), or which pages they go to (for outputs). It allows for a faster schematic walk-through, easier fan-out loading checks, and it makes the schematic set easier to read and follow. Inter-page signals must have different names from the I/O (off-chip) signal names.